Technical Brief: Bootstrap Trans-Impedance Amplifier for Large-Capacitance Photodiodes

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In a simple trans-impedance amplifier (TIA) circuit for a photodiode, the voltage noise at the output gets substantially larger as the photodiode capacitance increases. The increase of voltage noise gain with photodiode capacitance often goes unrecognized! This technical brief presents both the conventional simple TIA circuit and then another TIA that includes a "bootstrap" JFET to substantially reduce these effects.

Conventional simple high-gain TIA

: See *Figure 1*. The magnitude of the output voltage is essentially simply the photodiode output current times the feedback resistance (R_f). Two of the issues that exist for this circuit are high voltage noise gain (undesirable) and a relatively high gain bandwidth product (GBP) needed for the op amp. Other issues such as how to reliably achieve a very small C_f or a large R_f are discussed in other technical briefs.

1. Undesirably-High Voltage Noise Gain: The voltage noise gain of the *Figure 1* circuit is defined as the gain seen at the output due to op amp voltage noise referred to the positive input, $V_{gain} = 1 + Z_f / Z_{in}$. Here, $Z_f = 1/(sC_f) \parallel R_f$, and $Z_{in} = 1/ (s C_{Pd})$. So, $V_{gain} = 1 + [s R_f C_{Pd} / (s C_f R_f + 1)]$. A large R_f is highly desirable in terms of noise performance if the photodiode current is small, and a small C_f is necessary to achieve a relatively high bandwidth. However, one is then stuck with a relatively high voltage noise gain that is essentially set with the ratio of C_{Pd} / C_f.

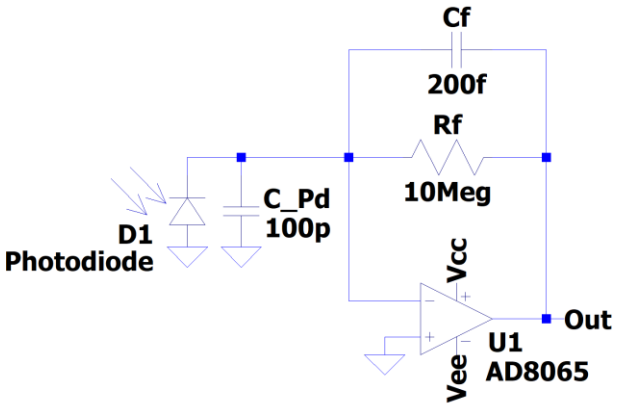

Figure 1: Conventional Simple High-Gain TIA (explicitly showing photodiode capacitance) The op amp has a 145MHz GBP.

Figure 2 shows what the noise gain looks like for 10pF and 100pF photodiode capacitances. Although these peak at different frequencies, the output with 100pF (red) peaks 19dB higher than the output with 10pF (blue)—allowing over 8.9 times more noise gain!

By the way, you might ask what causes the magnitude response to roll off at higher frequencies at 20dB/decade. The equation for V_{gain} above is one (0dB) at low frequencies, then has a zero due to C_{Pd} (causing a 20dB/decade rise), and then has a pole due to Cf around 100kHz (causing the response to level out). You'll see this if you run a Spice sim with an ideal op amp. So, the roll-off above 100kHz is

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due to the frequency response of the op amp itself. Even though the AD8065 has a GBP of 145-MHz, the frequency response is reduced by the 55dB voltage gain near 100kHz. If an op amp doesn't have enough open loop gain at a given frequency, it won't be able to properly amplify difference of its inputs. See page two of *Building Stable Op Amp Circuits*.

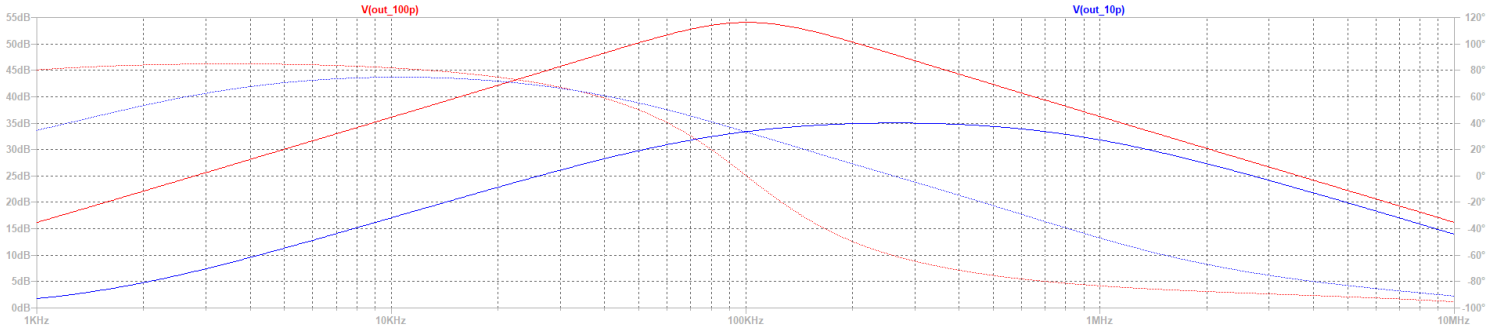

Figure 2: Voltage Gains of simple TIA with 10pF (blue) and 100pF (red) photodiode capacitances

Figure 3 shows the trans-impedance gains (current in to voltage out) of the circuit with 10pF (blue) and 100pF (red) photodiode capacitances. These trans-impedance gains are similar although the 100pF-circuit has a -3dB point at 111-kHz versus 90-kHz for the 10pF circuit. (One could lower C_f slightly in the 10pF circuit to achieve the same trans-impedance bandwidth as for the 100pF circuit.)

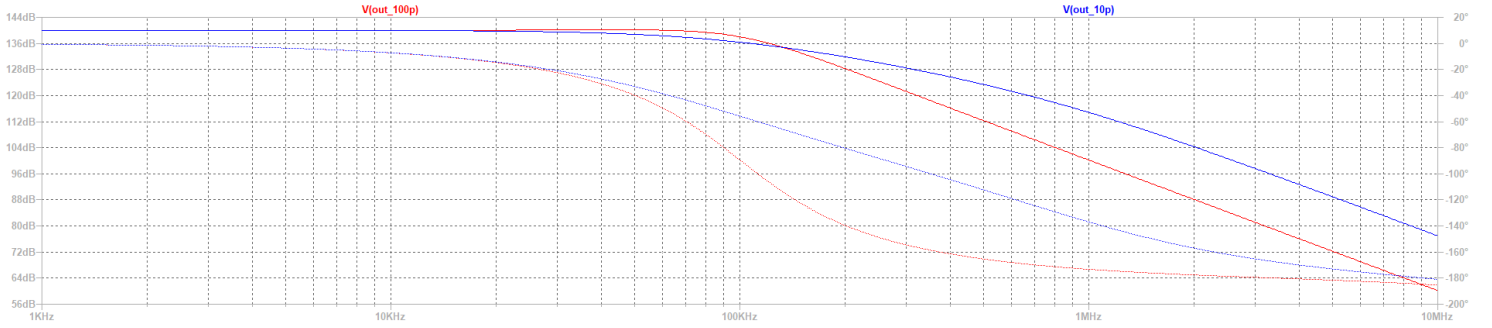

Figure 3: Trans-Impedance (Current to Voltage) gains of simple TIA with 10pF (blue) and 100pF (red) photodiode capacitances

Adding a Bootstrap JFET to high-gain TIA Input: See *Figure 4* below. In this circuit, positive photodiode current flows from +5V, through the JFET, into the photodiode cathode, through R_f (and C_f at higher frequencies) and into the op amp output (which goes more negative with increasing positive photodiode current). The JFET tends to conduct more current as its gate-source voltage goes from -5V towards 0V. The JFET operates here as a voltage follower or bootstrap to reduce the capacitance seen at the op amp inverting input mostly to the JFET's input capacitance (about 4pF for the one shown). The voltage at the photodiode cathode self-adjusts depending on the JFET's parameters, R2, and the power supply voltages (about 287mV for the values shown). However, the voltage from photodiode anode to its cathode voltage is always negative allowing the photodiode to operate as expected.

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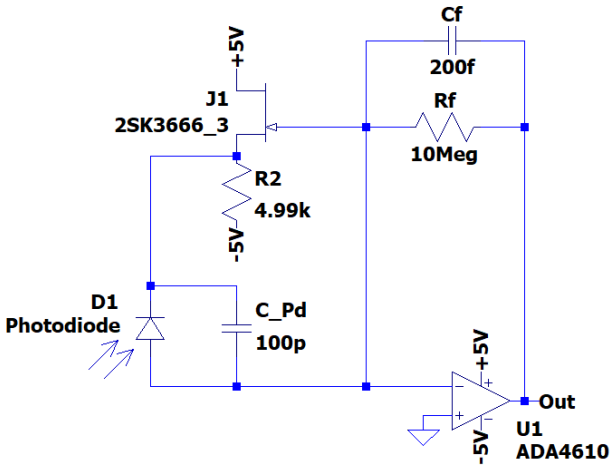

Figure 4: High-Gain TIA with JFET on Input (explicitly showing photodiode capacitance). The ADA4610 has a 15.4-MHz GBP.

Note that one can't simply reverse the connections of the photodiode in this circuit because then it will be forward-biased which tends to be undesirable for predictable performance. (Other topologies including with P-channel JFETs are probably also practical.)

The main disadvantages of this circuit are that it inverts the output compared to the *Figure 1* circuit, and more importantly, it has a negative offset at the output. This offset is approximately equal to the JFET gate leakage current times R_f (about 40mV here). The offset may not matter if one only cares about the AC content of the signal (which can be gotten rid of with an AC-coupling capacitor at the op amp output). Alternatively, one can add in a small positive offset at the non-inverting input of the op amp (e.g., with a DAC) or simply subtract the offset in software if the output is digitized.

The advantages of the TIA circuit with the bootstrap JFET are substantial in that it allows using an op amp with a GBP an order of magnitude smaller, and more importantly, **lowers the voltage noise gain**. This can be seen in *Figure 5* where the bootstrapped TIA with the 15.4-MHz op amp (C_{Pd} = 100pF) has about 19dB less noise gain than the simple TIA with the 145-MHz op amp (C_{Pd} = 100pF)! Also note that the bootstrap JFET with C_{Pd} = 100pF allows a similar reduction in voltage noise gain as reducing C_{Pd} from 100pF to 10pF in *Figure 1*. One can see from *Figure 6* that both of the TIAs roll off (-3dB) at about 118kHz.

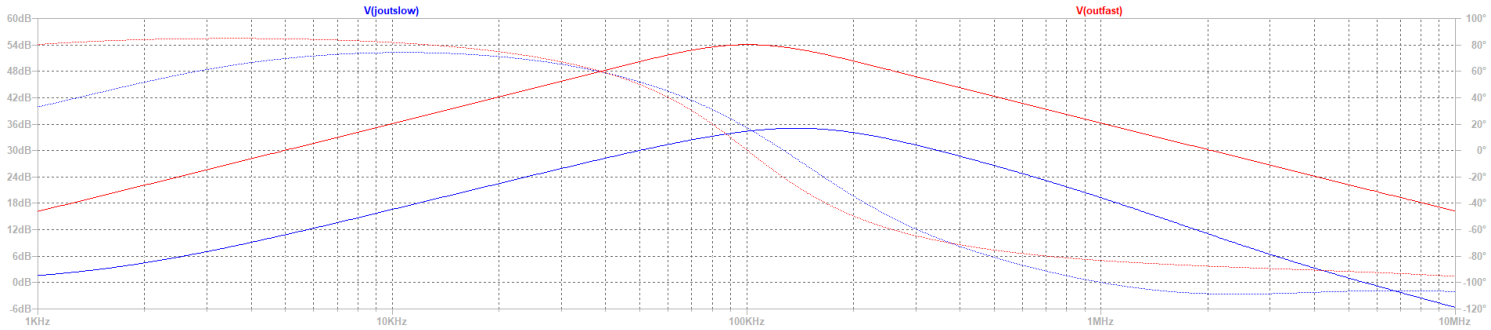

Figure 5: The red traces show the voltage gain of the simple TIA with a "fast" op amp (AD8065, 145MHz GPB) while the blue traces show the voltage gain of the TIA with a JFET and a "slow" op amp (ADA4610, 15.4MHz GBP). C_{pd} = 100pF in both cases.

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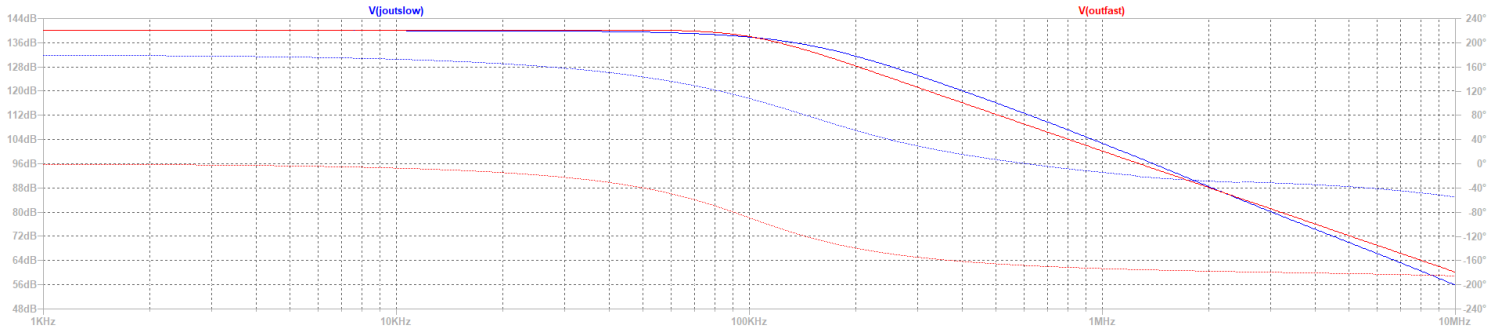

Figure 6: The red traces show the current gain of the simple TIA with a "fast" op amp (AD8065, 145MHz GPB) while the blue traces show the current gain of the TIA with a JFET and a "slow" op amp (ADA4610, 15.4MHz GBP). C_{pd} = 100pF in both cases.

Using an op amp with lower GBP may be more tolerant of compromises in the PCB layout since all things being equal, it will probably be less prone to oscillate due to stray capacitances, etcetera.

The usual advice of simulating the circuit before building it applies. Also, please see *Ultra low noise high bandwidth transimpedance amplifiers* for further ideas.

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