BÉLA A. GÉCZY

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ELECTRICAL ENGINEER

I strive to achieve quality, performance and reliability in the designs I produce. I believe a sound understanding and application of engineering principles is of the utmost value. I am a results oriented engineer with close to 20 years experience in analog design and construction. I have multi-disciplinary versatility including superb trouble-shooting and analytical skills to pinpoint and resolve potential errors in the early stages of design to avoid excess time/cost expenditures. Estimate, design, schedule, and oversee all phases of new construction from initial conception through successful startup. I am an excellent communicator and team player with success in coordinating efforts within teams to reach and surpass expectations.

Core Competencies:

- Analog Hardware Design
- Circuit Modeling and Simulation
- Circuit Prototyping
- Troubleshooting
- Printed Circuit Board Layout & Design (Mentor Graphics PADS)
- Engineering Documentation
- Cost Effectiveness Awareness
- Proficient with Multitude of Laboratory Test Instruments
- Research and Development
- Sales and Marketing
- Customer Service

PROFESSIONAL EXPERIENCE

REDGARDEN ENGINEERING, Boulder, CO — December 2012 – Present
Electronics Engineer

Continuing work includes analog and digital hardware design and PCB design. Design of high end audio amplifiers (voltage and current mode feedback), successfully designed and built and tested 15A current injection amplifiers for data communication through the power grid.

ENGINEERING CONSULTANT, Boulder, CO — May 2008 – February, 2011
Consultant

Consulting in electronics engineering utilizes my skills in analog and digital hardware design and PCB design. Work included high-energy battery chargers, a 10-A, 135-kHz sine wave driver design, EMI reduction, schematic and PCB design, and quality system documentation.

DHARMA INVESTMENT GROUP, Boulder, CO — Mar 2005 – Mar 2008
President

Investment company servicing over 250 clients. Principal duties included sales, marketing, customer service, contracts, accounting and finance.

MOUNTAIN ENGINEERING II (A consulting company), Longmont, CO — Aug 1989 – Feb 2005
Senior Analog Engineer

- Designed and implemented full Read/Write channel on Echo 8418, 8436 and 8436Fast tape drive. This consists of Magneto-Resistive Read Bias, Pre-Amplifier, AGC, Filters and Equalization, Phase Lock Loop, and Decoded Digital Data circuits. Also included are high speed Current mode Write Driver circuits for Inductive Write Heads.
- Designed Read/Write channel on Overland Data Inc.'s L490 1/2 inch tape drive
- Designed and implemented a novel proprietary Phase Lock Loop Integrated Circuit
- Designed and implemented 1/2 tape verification/certification test system for a large tape manufacturer
- Designed and implemented a low cost, high accuracy optical sensor test system that performs non-contact displacement measurements especially suitable for measurements of tape edges
- Responsible for design of a variety of customer desired linear circuits
- Extensive PCB design experience using Mentor Graphics PADS

- Small company experience requiring the wearing of many "hats" such as managing cost effectiveness in designs, time, and parts/equipment procuring; PBC design; PCB & mechanical assembly; soldering; documentation control; customer support; sales & marketing; etc.

ASPEN PERIPHERALS, Longmont, CO Sep 1986 – Aug 1989
Read/Write, LSI Group
Engineer III

- Designed and implemented full Read/Write channel on Aspen Peripherals A480 – the first available OEM 3480 1/2 inch cartridge tape drive, and on Aspen Peripherals Summit, Marketed as the StorageTek 42xx.
- Designed, implemented, and layout of a bipolar analog Read IC (including: Read Head bias, preamplifier, AGC, self test circuits) for Summit
- Manager and mentor for technicians

NATIONAL SEMICONDUCTOR, Santa Clara, CA Oct 1983 – Jul 1986
Linear Integrated Circuit Group
Assistant Engineer

- Responsible for Mask Design on National's proprietary VIP dual high speed NPN and PNP Bipolar process which included a combination of a high speed Op Amp plus Buffer
- Designed the hardware and software for automated A.C. testing of fast Op Amps for use in engineering R/D
- Built, tested and debugged low noise and high speed and precision analog circuits and assisted in linear circuit design using SPICE and SNAP computer simulation programs.

COMPUTER SKILLS

Proficient in Windows OS, MS Office, MathCad, Various Spice Circuit Simulation Software, Cadence OrCad Schematic capture, Mentor Graphics PADS Logic and PADS Layout, Altium Schematic and PCB design, QuickBooks

ACHIEVEMENTS

- Patent:
  No. 5,095,310 issued on 10 Mar 92 for a full analog implementation of LOOP-WRITE-TO-READ (self testing feature) in a 3480 class, high performance tape subsystem
- Article for CommsDesign: "FPGA-Based DPLL Approach Delivers Wide-Lock Range"
- Article for Electronic Design: "200 MHz PNP Transistors Spawn Fast Analog Chips," by Monticelli, Wright, Small and Geczy. ED, August 21, 1986, page 111

Efficient Communicator:
- Written a number of non-technical instructional ebooks (available upon request).
- Taught introduction to Non-Violent Communication (see www.cnvc.org).
- Ability to interact with individuals at all levels of technical understanding and especially the ability to clearly convey complex information to non-technical people.

EDUCATION

De Anza College, Cupertino, CA., G.P.A. of 3.25

University of Berkeley Video Course – Paul Gray instructor.
1) Analysis and Design of Analog Integrated Circuits.
2) Advanced Analog Integrated Circuits.

U.S. Air Force, 1972 – 1976